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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,474	07/18/2003	Paolino Schillaci	856063.743	4573

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SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,474	SCHILLACI ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *14-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7 and 11-13* is/are rejected.

7)☒ Claim(s) *3-6 and 8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This office action responsive to communication filed 04/20/2004. Claims 1-13 and 19-34 are presented for examination. Claims 14-18 are subjected to the restriction requirement, and being withdrawn from further consideration.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

NOTIFICATION OF OBJECTION AND/OR REJECTIONS

Election of Species/Restriction

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I. Claims 1-13, drawn to a decoding method for selecting a nonvolatile memory utilized the comparison approach wherein the comparison is performed in a LPC decoding block, classified in Class 711, subclass 1.

Group II. Claim 14-16, drawn specifically to a nonvolatile memory device having plurality of FLASH memories, classified in Class 711, subclass 103.

The inventions are distinct, each from the other for the following reasons:

The invention of groups I and II are related as combination/subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, the invention of group I has separate utility such as a method for selecting/decoding different type of memory devices in the network environment, and is not limited for use with a nonvolatile memory device having plurality of FLASH memories of group II. Similarly, the invention of group II can be used as a memory storage device for storing data signatures for allowing/rejecting accessing to secured data in any computer system and is not restricted for use with the decoding method for selecting a nonvolatile memory utilized the comparison approach of group I. See M.P.E.P. § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification and recognized divergent subject matter, and because the search required for one group is not coextensive with the search required for the other groups, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Mr. David V. Carlson (Reg. No. 31,153) on December 07, 2005; a provisional election was made without traverse to prosecute the invention of group I,

claims 1-13. Claims 14-16 are therefore withdrawn from further consideration by the Examiner.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 C.F.R. § 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently-filed petition under 37 C.F.R. § 1.48(b) and by the fee required under 37 C.F.R. § 1.17(h).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2, 7 and 11-13 are rejected under 35 U.S.C. § 102(b) as being anticipated by Shiau et al. (USPN: 6,119,226); hereinafter Shiau.

As per claim 1, Shiau discloses the invention as claimed

including an automatic decoding method for mapping and selecting a nonvolatile memory device having a LPC serial communication interface, wherein the memory is equipped with a plurality of addressing pins and mounted on a motherboard together with other memories of the same type bidirectionally connected with a controller putting it into communication with a processor housed in turn on the motherboard (e.g. see abstract, column 2, lines 29 et seq. and figure 1) comprises a processor that compares the addressing pins of each memory with a portion of the addressing coding bits both to identify the addressing type to be used, top-down or bottom-up, and to determine which memory is polled by the controller for a given operation; for example, Shiau discloses the decoders for decoding address coding bits by inverting the high order address bits to identify whether the memory access request is in the first type or second type address protocol and to determine which memory array row in the first type is polled for certain operation (e.g. see column 5, lines 27 et seq., colum 10, lines 1-12);

As per claim 2, wherein the comparison is performed in a LPC decoding block (e.g. see column 2, lines 22 et seq.; column 10, lines 7-12).

As per claim 7, Shiau discloses a non-volatile memory integrated device equipped with an interface with LPC serial protocol and a plurality of addressing pins in order to be

mounted on a motherboard together with other memories of the same type bidirectionally connected with a controller putting it into communication with a processor housed in turn on the motherboard (e.g. see column 2, lines 29 et seq.; column 6, lines 25 et seq.) wherein the processor contains in the LPC interface a logic identification structure both of the memory and of the addressing type to be used, top-down or bottom-up (e.g. see column 2, lines 38 et seq.); and the logic structure contains a comparator to compare a portion of the addressing coding bits with the addressing pins; for example, Shiau discloses the decoders for decoding address coding bits by inverting the high order address bits to identify whether the memory access request is in the first type or second type address protocol and to determine which memory array row in the first type is polled for certain operation; Shiau clearly discloses the logic is located within the decoder to decode a memory access request for boot code to the appropriate location in the array (e.g. see column 2, lines 58-64; column 5, lines 27 et seq., colum 10, lines 1-12);

As per claim 11, it encompasses the same scope of invention as to that of claims 1 and 7 except that it is drafted as method format rather than apparatus format, the claim is therefore rejected for the same reasons as being set forth above.

As per claims 12 and 13, the further limitation of sending a reset pulse if the identification signals do not indicate a

unique decoding scheme and there is not a direct match between the enabling signal and the bits residing on addressing pins of the memory circuit is taught by Shiau as addresses received from a processor implementing a T-type protocol will not be converted and therefore address protocol unit 136 output a logic 0 level signal (e.g. see column 7, lines 46 et seq.);

Allowable subject matter

8. Claims 3 and 8 are objected to as being dependent upon a rejected base claims 1 and 7; repestively, but would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. Claims 4-6 and 9-10 are also allowable since they are depended on the indicated allowable claims 3 and 8.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-41287. The examiner can normally be reached from 6:30 A.M. to 4:00 P.M.

If attempts to reach the examiner by telephone are

unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/December 07, 2005

Tuan V. Thai

PRIMARY EXAMINER

Group 2100